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A SOFTWARE-DEFINED RADIO APPROACH TO SPECTRUM SENSING SYSTEMS' ARCHITECTURE

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Abstract: *Software-Defined Radios (SDR) have developed exponentially in recent years. This is due to the high versatility that SDR platforms bring to communications systems. This survey aims at designing, developing, and validating a SDR-based Cognitive Radio Sensing System with a very high functionality to cost ratio. A Radio Band Power Measurement System will be implemented, as a proof of concept, which will perform Energy Detector sensing involving apriori knowledge of the target signal characteristics. Thus, it will identify available 6, 7 and 8 MHz Digital Terrestrial Television (DTT) channels. The reliability and reconfigurability of the prototype reveal the added value that our approach brings to Spectrum Sensing.*

Key words: *Spectrum Sensing, Software Defined Radio, Energy Detection.*

1. Introduction

It has become apparent that the severe underutilization of the electromagnetic spectrum [13] calls for alternative and novel solutions in the utilization of the radio resource. The process of statistically gathering and interpreting data to provide spectrum management information is called Spectrum Sensing. This technique requires reconfigurable hardware platforms and high processing power. An optimum solution is Software Defined Radio (SDR) Platforms.

1.1. Spectrum Sensing

A standard for a Cognitive Wireless Regional Area Network (WRAN) is being developed by the 802.22 working group, which will exploit unused DTT channels and provide fixed wireless access services. It is expected that the final standard will support 6, 7 and 8 MHz channels. The standard's draft form can be found in [16].

Sensing involves the analysis of the radio frequency spectrum and identifying unused spectrum for use by the WRAN [4].

The type of sensing used by the authors in this paper is called Energy Detector, a blind sensing technique that does not rely on any special signal features detection (i.e. correlation).

1.2. Energy Detector Sensing

Energy detector (power detector) sensing computes an estimation of the signal power in the considered channel and compares

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the resulting indicator to a predefined threshold [7].

Energy Detectors employ Fast Fourier Transform (FFT) frequency bins averaging, similar to the functionality of a traditional spectrum analyzer [1].

The energy detectors' primary user detection threshold is known to be highly susceptible to time-variable noise levels. Also, this sensing solution does not provide a way for discriminating between the desired modulated signals, noise or interference. It is for this reason that energy detection does not work for spread spectrum signals sensing (direct sequence or frequency hopping signals), and hence, different types of spectrum sensing techniques must be approached [6], [1].

1.3. Software-Defined Radio

The novelty of the sensing system, described in this manuscript, is the integration of software and programmable hardware, in particular a SDR platform in order to implement a communication system.

A SDR system is made up of a SDR hardware platform and its associated software framework and functionality.

The term Software Defined Radio was coined in [3] by J. Mitola, and described as being the process of building digital communications systems by employing general purpose hardware and pairs of digital to analog (DAC) and analog to digital converters (DAC and ADC) for digital signal processing.

GNU Radio founder Eric Blossom, states in [11] that SDR is a means of getting the programming "as close to the antenna as possible" so as to turn "radio hardware problems into software problems" which are more flexible and manageable. SDRs digitally handle the generation of a signal and its modulation/demodulation and transmission/reception processes.

To sum up, a SDR communication module is capable of dynamic reconfigurability. Its functionality range is extended by its ability to operate on multiple frequency bands over an ample radio spectrum sweep [5].

2. Sensing System Architecture

A typical SDR based Cognitive Radio Sensing System architecture and its functional blocks are depicted in Figure 1.

The SDR Hardware Platform is usually comprised of the Radio Frequency Front-End and the SDR MotherBoard Blocks.

The RF Front-End gathers the signal from the antennae, after which it filters, amplifies and tunes the signal to a baseband frequency dependent on the board's IF bandwidth and local oscillator frequency [15].

The signal is next directed to the SDR Motherboard block. Here, digital samples of the analog signal are formed by the analog-to-digital converter (ADC). The values of the digital samples are then forwarded towards the FPGA where digital down converters (DDC) ensure that the output signal will have the specified frequency and sample rate [11]. The I and Q paths derive from the multiplication of the samples with sine, respectively cosine, function. Next up is the decimation stage, which implies a decimation by an externally defined arbitrary factor, N. The resulting signal is the SDR platform's output signal towards the host side [15].

While able to perform basic digital signal processing (DSP), with its General Purpose Processors and FPGAs, the SDR platform's limited processing capabilities require the processing power of the Host Computer Block. This is usually a personal computer (PC) with sufficient processing power, able to run the appropriate software. The System Software Block is a collection of explicit DSP software, capable of implementing sensing-specific statistical algorithms and functional flows. This block is run by the Host Computer.

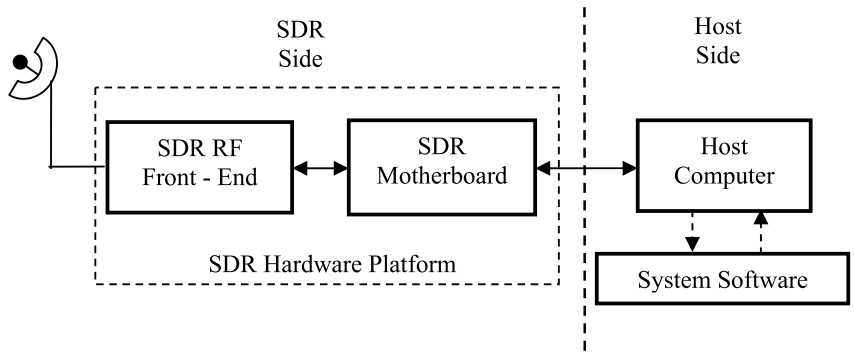

Fig. 1. *Functional flow of a SDR based Cognitive Sensing System*

2.1. Software Defined Radio Platform

SDR hardware platforms were studied as to determine the optimum candidate concerning the required, functionality to cost ratio. The first term, functionality, indicates that the proposed system clearly satisfies its purpose, namely agile spectrum sensing in order to identify unused radio channels. The second term of the ratio, cost, implies that, as long as the functionality of the system is satisfactory, it should remain to a minimal value.

Table 1 portrays the differential analysis for available RF front end solutions.

According to the "functionality to cost" paradigm, it clearly emerges from Table 1, that the optimum solution is Ettus Research's platform, entitled Universal Serial Radio Peripheral 2 or USRP2.

In USRP2s, ADCs have a dynamic range of 14 bits and a sampling rate of 100 mega samples per second (MS/s).

Towards the host side, USRP2 uses the Gbit-Ethernet connection, allowing for a high throughput. The theoretical (complex) radio frequency (RF) bandwidth is of about 31.25 MHz, although the usable bandwidth has a limit of 25 MHz.

USRP2 daughterboards are RF front ends that plug into one of four sockets on the motherboard and are each designed to support and operate over a wide range of different radio frequency bands. Analog components on these boards upconvert, downconvert and amplify the IF signals to the desired RF and broadcast the output signal [15].

The daughterboard that we use in this paper is called WBX and it is a 50 Hz to

Differential Analysis of SDR Front Ends Table 1

Name	Year	RF bandwidth [MHz]	Processing	Processing Architecture	Connectivity	No. of antennae/Tx paths	Cost [$]
USRP	2005	8	Offboard	GPP	USB2	4	700
USRP2	2008	25	Mixt	GPP, FPGA	GigEthernet	2	1400
BEE2	2007	25	Onboard	FPGA	USB, Ethernet	16	20000
LYRTECH	2006	5, 7, 20 or 20	Onboard	GPP, FPGA	Ethernet	2	9900
FLEX 3000	2005	0.048	Offboard	GPP	Firewire	2	1599
WARP	2008	24	Onboard	FPGA	SATA, HSSDC2	4	6500

2.2 GHz transceiver with applications in such transmission fields as DVB-T, GSM, or GPS [12].

2.2. Sensing System Software

Initially, two options were considered as solutions for the developed prototype.

The first is called GNURadio, an open source framework for software radios that offers application interface (API) functionalities for USRP2 users.

Due to its limited functionality and support in comparison to other similar solutions, GNURadio was dismissed as potential solution for the time being.

Scenarios of Matlab to GRC interactions were implemented, as an indirect functional flow between Matlab and USRP2, with moderate success, however, because of GRC's limited development and functionality [14].

When trying to develop a Software Defined Radio Sensing Prototype, Matlab, with its extensive DSP capabilities, is the software framework of choice. As of September 2010, Simulink - USRP2 interaction is natively supported by the newly launched Matlab 2010b.

Simulink's USRP2 Receiver block enables data transmission, inside the same Ethernet subnetwork, towards the USRP2 board [18].

The communication between the two entities is done through User Datagram Protocol (UDP) packets. The USRP2 Receiver block yields an output column vector signal of fixed length and format (358x1). Some of the USRP2 parameters directly configurable through Simulink are central operating frequency, gain and decimation [18].

3. Experimental Setup and Results

As a proof of concept, for the proposed Sensing System architecture we have implemented a Radio Band Power Measurement System, capable of performing a coarse Energy Detector sensing upon Digital Video Broadcasting - Terrestial (DVB-T) channels, by using apriori knowledge of the target signal characteristics (i.e. frequency, bandwidth).

The system is comprised of a USRP2 SDR platform, with its antennae and WBX daughterboard which stand for the SDR Hardware Platform from Figure 1, and a 2.6 GHz (Intel Dual Core) processor, 2 Gb RAM memory, computer which is represented by the Host Computer block in Figure 1. The computer's operating system is Linux Ubuntu 10.04 Lucid, while the specialized DSP specific software used is Matlab 2010b framework's Simulink. The latter two components constitute the System Software block from the general SDR based Sensing System architecture from Figure 1. For testing purposes and precision estimations, parallel measurements were carried out with a Signal Generator and a Vector Spectrum Analyzer (VSA) from Agilent Technologies [8]. UDP protocol specific FPGA and Firmware images were used for ensuring the USRP2 module's compatibility with Simulink.

3.1. DVB-T Power Measurements

The System Software Block from Figure 1 is the core of the entire proposed Sensing System. It is here that all the radio spectrum data is collected by the SDR platform, ordered and interpreted according to the sensing algorithm. In this experimental implementation we have chosen to utilize the Energy Detector algorithm, which is, in fact, a Fast Fourier Transform (FFT) coefficient based, power measurement. In Figure 2, the Simulink functional flow of this process is shown.

The USRP2 Receiver block is where USRP2 functional parameters can be modified, even during execution. With the help of Slider blocks, Central Frequency, Decimation and Gain can be adjusted. The USRP2 block needs the broadcast static IP, 192.168.10.255.

In order to preserve an accurate and coherent graphic representation of the acquired signals the sample time has to respect the following implication:

$$S_T = \frac{M}{R}, \qquad (1)$$

S_T is the Sample time, M is the decimation rate, R is USRP2's ADC conversion rate.

In this case, as the decimation rate has a value of 12, the sample time will be 12 x 10^{-8} s. The decimation value is restricted between a minimum of 4 and a maximum of 512, and needs to be a multiple of 4.

The elements of the USRP2 module's output vector are of type floating point with double precision, with 358 x 1 format.

By implementing parameter values of: *Gain* = 0 dB; *Central Frequency* = 646 Mhz; *Decimation* = 12; we will get a 358 x 1 output vector that represents a frequency baseband of 8.33 MHz, with a central frequency of 646 MHz.

Parallel measurement, conducted with a VSA, revealed that 646 MHz is the central frequency of an 8 MHz DVB-T channel. This is the previously mentioned apriori knowledge of the sensing's target signal characteristics.

Because of the difference in bandwidth, between a DVB-T channel and the 0.33 MHz gathered baseband, an additional "trimming" stage is necessary. The Rational Resampler block, in Figure 2 implements, alongside a specific Finite Impulse Response (FIR) filtering process, a resampling of the 8.33 MHz baseband, with a fractional factor of 24/25, to the size of a DVB-T channel, 8 MHz.

Since the USRP2 vector's native format is 358 x 1, an unbuffer - buffer operation is required in order to have a. format. This is due to the fact that FFT blocks only accept power of 2 formats. Consequently, we will have an Unbuffer block, followed by a 2048 Buffer block. The effect is that the signal vector, now has a format of 2048 x 1.

The Magnitude FFT block provides the functional flow with the magnitude

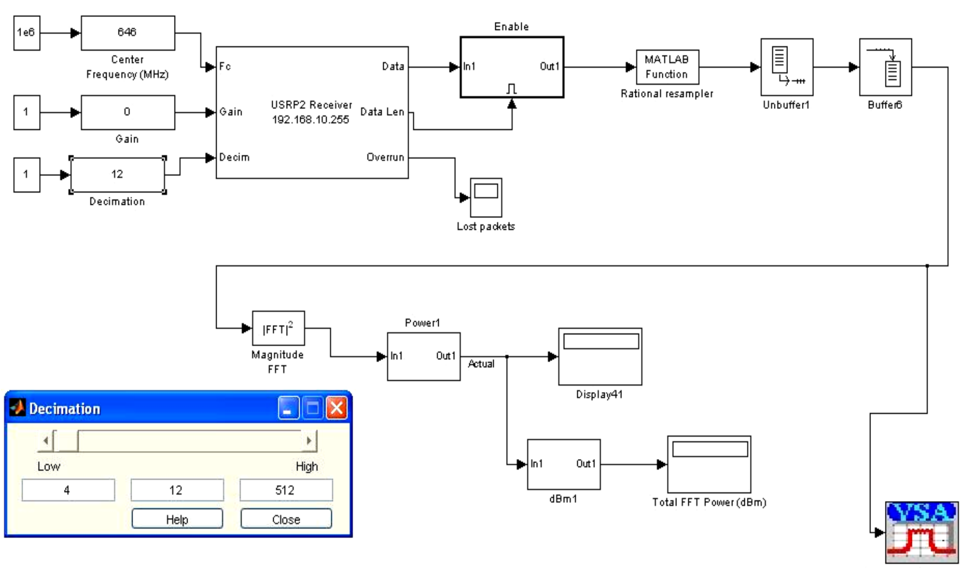

Fig. 2. *Functional flow of the implemented Sensing System*

coefficients of the input signal as a result of FFT. The subcomponents of the block are available at [17].

The output is a number of 2048 squared FFT coefficients of the input signal.

The resulting coefficients are utilized in computing the band power value [9] by using the authors' algorithm that is implemented in the Power custom block.

The determined Band Power value is then transformed into [dBm], decibels referenced to 1 mW, in the block named dBm (Figure 3).

The following mathematical expression reflects the functionality of the dBm block:

$$x = 30 + 10\log_{10} P, \qquad (2)$$

where P is the power ratio expressed in watts and x is the power ratio in [dBm].

Parallel to the authors' Sensing System, an array of control power measurements were made by means of an Agilent 86900 high-precision VSA connected within the same subnetwork with the host, which communicates directly with a VSA block [8]. The test point was the output of the Buffer block (input of the Magnitude FFT block) from Figure 2.

Multiple measurements over the course of several days and over a variety of, bandwidths, spectral domains and conditions have proven that the results from the two scenarios differ by a maximum of 0.7%, which validates our prototype and our premises.

3.2. Power Measurement Algorithm

According to [2] band power is directly proportional with its magnitude. The Magnitude FFT block, computes 2048 FFT coefficients and squares them, in order to obtain the 2048 magnitude coefficients of an 8 MHz frequency band. These parameters are passed then towards the input of the Power block. This is where the value of the DVB-T channel power is computed. Figure 3 portrays the functional flow of this block and its subcomponents.

As indicated by [9] an Agilent VSA (i.e. 35670 A) computes the band power by summing up all the squared FFT coefficients, and dividing the sum to the effective bandwidth. The effective bandwidth is the result of the division of the frequency span to the number of FFT bins and subsequent multiplication by the window factor. The windows factor value is 1 for uniform windows, 3.82 for Flat-top windows or 1.5 Hanning.windows.

The authors used a formula similar to the one that Matlab uses to compute vector signals power [10]:

$$P = 10\log_{10} \cdot \sum Coef_{FFT}^{2} \cdot \frac{Window_{fact} \cdot Freq_{Span}}{N_{FFT} \cdot \mathrm{Re}\, z_{Band}}. \qquad (3)$$

As a result of multiple tests and trials a fully functional optimized algorithm for computing the DVB-T channel power value was developed (Figure 3).

The first block after the input is a FIR filter, used for suppressing non-linearities related to the FFT squared coefficients. Next up, is a Sum block. The resulting sum is divided by the number of squared FFT coefficients, but also by 2 ($\sqrt{2}$ squared) as to obtain RMS values. A division by the value of the buffer is also necessary. A division by 50 Ohm, the value of the radio characteristic impedance is the last step before finding the channel power value in [µW].

4. Conclusions and Future Development

In this paper the authors designed and developed a SDR based Cognitive Radio Sensing System with a very high functionality to cost ratio. The authors then

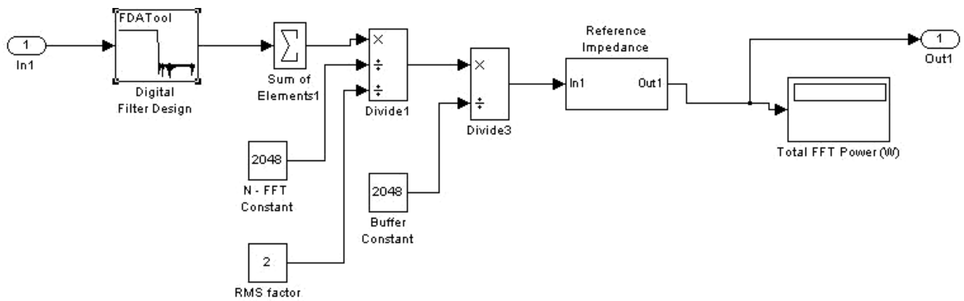

Fig. 3. *Functional flow of the implemented Sensing Algorithm*

proceeded to validate this prototype by implementing a Band Power Sensing System based on the concept of Energy Detector Sensing, which proved to provide significant added value from the functionality to cost ratio point of view, when compared to traditional sensing architectures and systems.

The implementation solution that the authors have opted for, was a functional flow based on the developed general sensing prototype. The chosen SDR platform was Ettus Reasearch's USRP2, while the DSP software opted for was Matlab 2010b's Simulink. It was in this software that the Energy Detector sensing functional core was implemented.

As further developments, the authors considered improving the Energy Detector sensing method from the functionality and precision point of view, by using methods such as channel discrimination by Wavelet Packet Decomposition or feature detection. This would be done with no additional hardware modifications to the prototype's architecture which is the quintessential advantage of using SDR platforms.

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